TE. (Sem-VI) Course: Processor Organization and Architecture (DJ19CEC502)

|  |  |  |  |
| --- | --- | --- | --- |
| Q 1. (a) | Compute (-16)\*(-29) using Booth’s Multiplication Algorithm. | [05] | CO1 |
| OR | | | |
| (b) | Compute (-15)\*(-29) using Booth’s Multiplication Algorithm. | [05] | CO1 |
| Q 2. | Derive the formula for Computing Average Memory Access Time for the given virtual structure of memory interfacing. Also compute it.  MM  L1  Processor  L2  Assume TLl=15ns, TL2=18ns, TMM=1225ns, HL1=75%,HL2=95%, HMM=65%. Find Average Memory Access Time. | [10] | CO2 |
| Q 3. | Differentiate between Von Neumann and Harvard Architecture | [05] | CO1 |
| Q.4.(a) | Given Computer System has a 32-bit addresses. Each block stores 16 words. A direct-mapped cache has 256 blocks. In which block (line) of the cache would we look for each of the following addresses? Addresses are given in hexadecimal for convenience.  a. 1A2BC012                   b. FFFF00FF | [05] | CO2 |
| OR | | | |
| Q.4.(b) | A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.  (a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address. | [05] | CO2 |

**ALL THE BEST!**